IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A method performed in an error correction system, the method comprising the steps of:

determining if an actual number of errors is less than a maximum error correction capability; and

reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability.

2. (Original) The method of claim 1, wherein the step of reducing power consumption further comprises the step of gating one or more clocks coupled to the error correction system.

3. (Original) The method of claim 1, further comprising the step of providing a plurality of intermediate polynomials, and wherein the step of reducing power consumption in the error correction system when the actual number of errors is less than the maximum error correction capability further comprises the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree.

4. (Amended) The method of claim 3, wherein one intermediate polynomial is a first error evaluator polynomial $R(x)$, wherein one intermediate polynomial is a first error locator polynomial $F(x)$, wherein $R^{(r+1)}(x) = F^{(r+1)}(x) \cdot S(x) \bmod x^{2t}$, wherein r is a number of iterations, $S(x)$ is a syndrome polynomial, and t is a number of errors capable of being corrected, wherein one intermediate polynomial is a second error evaluator polynomial $Q(x)$, wherein one intermediate polynomial is a second error locator polynomial $G(x)$, wherein $Q^{(r+1)}(x) = G^{(r+1)}(x) \cdot S(x) \bmod x^{2t}$, ~~and~~ wherein the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree further comprises the step of determining if a degree of either $R(x)$

or *Q(x)* is less than a predetermined degree, wherein *R(x)* and *F(x)* are valid when a degree of *R(x)* is less than the predetermined degree, and wherein *Q(x)* and *G(x)* are valid when a degree of *Q(x)* is less than the predetermined degree.

5. (Amended) The method of claim 3, further comprising the step of providing, in the decoder, a plurality of intermediate polynomial elements and a calculation circuit coupled to the intermediate polynomial elements, each intermediate polynomial element containing coefficients of one of the intermediate polynomials, and wherein the step of reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability further comprises the step of placing a predetermined state into each of the intermediate ~~polynomials~~ polynomial elements, the predetermined state selected to reduce switching of the calculation circuit.

6. (Original) The method of claim 5, wherein the predetermined state is zero.

7. (Original) The method of claim 1, further comprising the steps of:
determining a plurality of syndromes;
determining if all of the syndromes have a predetermined value; and
reducing power consumption of the decoder of the error correction system when all of the syndromes have the predetermined value.

8. (Original) The method of claim 7, wherein the predetermined value for each syndrome is zero.

9. (Original) The method of claim 7, wherein the method further comprises the steps of providing a key equation solving device in the decoder, and providing a plurality of syndrome generators, each of the syndrome generators determining one of the syndromes, wherein the key equation solving device is coupled to each of the syndrome generators, and wherein the step of reducing power consumption of the decoder of the

error correction system when all syndromes have the predetermined value further comprises the step of not enabling the key equation solving device when all of the syndromes have the predetermined value.

10. (Original) The method of claim 9, further comprising the step of calculating at least one error polynomial when at least one syndrome does not have the predetermined value.

11.-24. (Withdrawn)

25. (Original) A decoder comprising:

means for determining if an actual number of errors is less than a maximum error correction capability; and

means for reducing power consumption in a decoder of an error correction system when the actual number of errors is less than the maximum error correction capability.

26. (Original) An integrated circuit comprising:

means for determining if an actual number of errors is less than a maximum error correction capability; and

means for reducing power consumption in a decoder of an error correction system when the actual number of errors is less than the maximum error correction capability.

27. (Withdrawn)